REMARKS

Claims 1-5 and 12-16 have been cancelled, mooting their rejections. Applicants respectfully traverse the remaining claim rejections. Before addressing the particulars of the claim rejections, Applicants note the following features for embodiments of their inventive integrated inductor. For example, as seen in Figures 3a, 3b, and 4, consecutive metal layers are used to form coils of an integrated inductor. Each layer includes at least two complete coil turns. So that the magnetic flux from each coil will add, there is an alternating arrangement of vias between layers – for example, consider the two layers 302d and 302e in Figure 4, where the outer ends of the corresponding coils are coupled through a via. However, from element 302e to element 302f, the inner ends are coupled through a via. In that fashion, a current flowing into port 1 will follow a clockwise path as it spirals into the inner radius 110a in layer 302f. This same clockwise path will be followed as the current spirals through the remaining layers until it reaches port 2. In this fashion, if there are N layers, the overall inductance will increase by N^2 as discussed in paragraph 53. Thus, not only is a very compact design enabled by this arrangement of vias but the inductance is increased as well. But this is not the only advantage -- note that port 2 will couple to the outer radius of layer 302a adjacent the substrate. As discussed, for example, in paragraphs 40 and 41, this bottom port is closest to the substrate and would thus have a higher capacitive interaction with the substrate. But this port may be coupled to a power supply as ground to avoid this capacitive loading. In this fashion, a compact but high Q inductive design is achieved.

Claim 6 has been amended to reflect these advantageous features. No new matter is added. As amended, claim 6 recites "a semiconductor substrate; a plurality of

conductive layers formed on the substrate, the plurality of conductive layers being arranged from a first conductive layer closest to the substrate to a last conductive layer furthest from the substrate; and a plurality of conductive spirals corresponding to the plurality of conductive layers such that a first spiral is formed in the corresponding first conductive layer, a second spiral is formed in the corresponding second conductive layer, and so on, wherein each spiral includes at least two concentric turns coiled from a first end at an outer radius of the spiral to a second end at an inner radius of the spiral; wherein the first end of the first spiral forms a first port for the inductor, a second end of the first spiral couples through a first via to the second end of the second spiral, the first end of the second spiral couples though a second via to the first end of the third spiral, and so on such that the second end of the next-to-last spiral couples through a last via to the second end of the last spiral, the first end of the last spiral forming a second port for the inductor." In this fashion, claim 6 recites an alternating via arrangement as discussed above, an arrangement which leads to a "right hand rule" of current flow in that if the current through a given spiral is clockwise, so it shall be in the remaining coils. Similarly, if the current through a given spiral is counter-clockwise, so will the current flow be in the remaining spirals.

The cited prior art stands in sharp contrast. For example, consider the Merrill reference (USP 5,610,433), which discloses a layered integrated inductor. However, unlike the advantageous flux-reinforcing and compact arrangement recited in claim 6, the spirals in each layer do not form continuous multiple turns. Instead, as seen, for example, in Figure 1 of Merrill, coil 12 does not form a spiral with the coil 44 in the same layer. Instead, coil 12 couples to coil 20 in the adjacent layer. Similarly, coil 44 couples to coil

42 in the adjacent layer. Thus, Merrill must have two vias between each layer, thereby adding to manufacturing complexity and cost. Accordingly, claim 6 is patentable over the Merrill reference.

The Berthold reference (USP 6,717,503) adds nothing further. Indeed, Berthold merely uses two metal layers to form a spiral that runs parallel to the substrate surface as seen, for example, in Figure 2 (metal layers 1 and 4 are used). No suggestion or teaching is thus made for the stacked structure recited in claim 6.

Finally, the Yamazaki reference also adds nothing further. As with Berthold, Yamazaki teaches only the use of two metal layers (see, e.g., Figures 6a, 6b, 7a, 7b, 9a, 9b, and 10a-f). No suggestion or teaching is thus made for the stacked structure recited in claim 6.

Claims 7 through 11 depend either directly or indirectly upon claim 6 and are thus patentable over the art of record for at least the same reasons. Support for the "each turn of each spiral comprises five or more linear segments" limitation of claim 7 may be seen in paragraph 45. Advantageously, implementing each turn using linear segments makes for more convenient photolithographic formation of the turns. Claims 8 and 9 have been amended responsive to the amendments to claim 6. Claim 10 has been amended to limit the turns of claim 7 to be eight, support for which is seen in paragraph 45. Finally, claim 11 has been amended to have the first port (closest to the substrate) be coupled to a power supply as discussed above and in paragraphs 40 and 41.

Several typographical and grammatical errors in the specification has been corrected. No new matter was added.

CONCLUSION

For the above reasons, pending Claims 6 – 11 are in condition for allowance and allowance of the application is hereby solicited.

If the Examiner has any questions or concerns, a telephone call to the undersigned at (949) 752-7040 is welcomed and encouraged.

Certification of Facsimile Transmission
I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Linda Bolter — October 28, 2004
Linda Bolter — Date of Signature

Respectfully submitted,

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